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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,500	ADILETTA ET AL.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/8/03 & 4/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1 Claims 21-35 are presented for examination.

2 The numbering of claims is not accordance with 37 CFR § 1.126. The original numbering of the claims must be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When claims are added, except when presented in accordance with 37 CFR § 1.121(b), they must be renumbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 38-52 have been renumbered 21-35, respectively.

3 In applicants PTO-1449 form filed April 26, 2004, reference ASSS and ASSSSSS have not been considered because the citation cites the identical patent number from citation ARRR and ARRRRRR respectively while listing a different patentee. Since it is not known which patent applicant may have intended to reference, the correct citations (ARRR and ARRRRRR) have been considered and the incorrect citations (ASSS and ASSSSSS) have not been considered.

4 Claims 22-35 are rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

All of claims 22-35 as written depend upon parent claims that have been canceled. Accordingly, the dependent claims have no parent claims. However, for purposes of examination, the claim dependency will be interpreted based upon the following:

Indicated parent	Interpreted parent
1	21
3	23
8	28

9 29
11 31

4.1 The following terms lack proper antecedent basis:

4.1.1 "the plurality of microcontrol engines" claim 22, lines 2-3;

4.1.2 "the internal bus arrangement" claim 32, lines 1-2;

4.1.3 "the memory control system" claim 24, lines 1-2, claim 25, lines 1-2;

4.1.4 "the shared resources" claim 34, lines 1-2;

5 The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornam*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a Terminal Disclaimer. A Terminal Disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6 Claims 1-17 of patent 6,606,704 contain every element of claims 21-32 and 34-35 of the instant application and as such anticipate claims 25-32 and 34-35 of the instant application.

7 Claim 33 of copending application 09/473,571 contains every element of claim 21 of the instant application and as such anticipates claim 21 of the instant application.

8 Claim 16 of copending application 10/615,280 contains every element of claim 21 of the instant application and as such anticipates claim 21 of the instant application.

9 Claims 1-3 of copending application 10/684,078 contain every element of claims 21 and 23 of the instant application and as such anticipate claims 21 and 23 of the instant application.

10 Claims 24 and 27 of copending application 10/726,757 contain every element of claims 21 and 23 of the instant application and as such anticipate claims 21 and 23 of the instant application.

> "A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. *In re Longi*, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); *In re Berg*, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus." *Eli Lilly and Company v. Barr Laboratories, Inc.*, United States Court of Appeals for the Federal Circuit, on petition for rehearing en banc (Decided: May 30, 2001).

11 The claim anticipation can been see from the following tables:

U.S. Patent 6,606,704 - Claim 1	***Application 10/615,500 - Claim 21***
A	A
parallel hardware-based multithreaded	
processor comprises:	processor comprises:
a plurality of microengines that support multiple hardware threads,	a plurality of microengines that support multiple hardware threads.

U.S. Patent 6,606,704 - Claim 1	*Application 10/615,500 - Claim 21*
each microengine comprising: a plurality of program counters; with the microengines maintaining states associated with the program counters to enable a plurality of sets of threads of computer instructions to be simultaneously active on each of the microengines while one actually executes at any one time;	
a general purpose processor that coordinates system functions,	a general purpose processor that coordinates system functions; and
the general purpose processor loading microcontrol programs for the plurality of microcontrol engines; and a first bus to couple the general purpose processor to the plurality of microengines.	

U.S. Patent 6,606,704 - Claim 2	*Application 10/615,500 - Claim 23*
The processor of claim 1 further comprising a memory control system.	The processor of claim 21 further comprising a memory control system.

U.S. Patent 6,606,704 - Claim 3	*Application 10/615,500 - Claim 24*
The processor of claim 2 wherein the memory control system comprises a synchronous dynamic random access memory controller that sorts memory references based on whether the memory references are directed to an even bank or an odd bank of memory;	The processor of claim 21 wherein the memory control system comprises a synchronous dynamic random access memory controller that optimizes memory references based on whether the memory references are directed to an even bank or an odd bank of memory.
and a static random access memory controller that optimizes memory references based upon whether the memory references are read references or write references.	

U.S. Patent 6,606,704 - Claim 3	*Application 10/615,500 - Claim 25*

U.S. Patent 6,606,704 - Claim 3	*Application 10/615,500 - Claim 25*
The processor of claim 2 wherein the memory control system comprises a synchronous dynamic random access memory controller that sorts memory references based on whether the memory references are directed to an even bank or an odd bank of memory;	
and a static random access memory controller that optimizes memory references based upon whether the memory references are read references or write references.	The processor of claim 1 wherein the memory control system comprises a static random access memory controller that optimizes memory references based upon whether the memory references are read references or write references.

U.S. Patent 6, - Claim 4	*Application 10/615,500 - Claim 26*
The processor of claim 1 wherein each of the plurality of microengines	The processor of claim 21 wherein each of the plurality of microengines
use the program counters to	
enable hardware-based context swapping amongst the plurality of threads that are independently executable within each of the microengines.	employ hardware-based context swapping amongst a plurality of threads that are independently executable within each of the microengines.

U.S. Patent 6, - Claim 5	*Application 10/615,500 - Claim 27*
The processor of claim 1 further comprising an bus interface that couples the processor to a communication bus.	The processor of claim 21 further comprising a high speed bus interface that couples the processor to a communication bus.

U.S. Patent 6, - Claim 6	*Application 10/615,500 - Claim 28*
The processor of claim 1 further comprising a bus interface that couples the processor to a computer system bus.	The processor of claim 21 further comprising a bus interface that couples the processor to a computer system bus.

U.S. Patent 6, - Claim 7	*Application 10/615,500 - Claim 29*
The processor of claim 1 further comprising: an internal bus arrangement to couple shared resources in the processor to the plurality of microengines.	The processor of claim 21 further comprising an internal bus arrangement to couple shared resources in the processor to the plurality of microengines.

U.S. Patent 6, - Claim 8	*Application 10/615,500 - Claim 22*
A parallel hardware-based multithreaded processor comprises: a plurality of microengines that support multiple hardware threads, each microengine comprising: a plurality of program counters; with the microengines maintaining states associated with the program counters to enable a plurality of sets of threads of computer instructions to be simultaneously active on each of the microengines while one actually executes at any one time; a general purpose processor that coordinates system functions,	The processor of claim 21 wherein
the general purpose processor loading microcontrol programs for the plurality of microcontrol engines;	the general purpose processor load microcontrol programs in the plurality of microcontrol engines.
a media access controller device coupled to an interface; and a first bus to couple the general purpose processor, the plurality of microengines, and the interface.	

U.S. Patent 6, - Claim 9	*Application 10/615,500 - Claim 35*
A parallel hardware-based multithreaded processor comprises: a general purpose processor that coordinates system functions; and a plurality of microengines that support multiple hardware threads, the microengines comprising: a control store to store a microprogram; the microprogram loadable by the general purpose processor;	

U.S. Patent 6, - Claim 9	*Application 10/615,500 - Claim 35*
controller logic including an instruction decoder and program counter unit to execute the microprogram; and a plurality of program counters; with the microengines maintaining states associated with the program counters to enable a plurality of sets of threads of computer instructions to be simultaneously active on each of the microengines while one actually executes at any one time.	The processor of claim 1 wherein each one of the microengines includes a program counter to uniquely identify a position of a thread during execution in the microengine.

U.S. Patent 6, - Claim 14	*Application 10/615,500 - Claim 30*
The processor of claim 9	The processor of claim 29
further comprising an internal bus arrangement to couple shared resources in the processor to the plurality of microengines	
wherein the internal bus arrangement to couple shared resources, comprises:	wherein the internal bus arrangement to couple shared resources, comprises:
a translator device that translates requests from the general purpose processor to the microengines; and	
a first bus to couple the general purpose processor to the plurality of microengines; and	a first bus to couple the general purpose processor to the plurality of microengines.
a second bus to couple the general purpose processor to the memory control system.	

U.S. Patent 6, - Claim 14	*Application 10/615,500 - Claim 31*
The processor of claim 9	The processor of claim 29
further comprising an internal bus arrangement to couple shared resources in the processor to the plurality of microengines	

U.S. Patent 6, - Claim 14	*Application 10/615,500 - Claim 31*
wherein the internal bus arrangement to couple shared resources, comprises:	wherein the internal bus arrangement to couple shared resources, comprises:
a translator device that translates requests from the general purpose processor to the microengines; and	a translator device that translates requests from the general purpose processor to the microengines; and
a first bus to couple the general purpose processor to the plurality of microengines; and	a first bus to couple the general purpose processor to the plurality of microengines.
a second bus to couple the general purpose processor to the memory control system.	

U.S. Patent 6, - Claim 14	*Application 10/615,500 - Claim 32*
The processor of claim 9	The processor of claim 23
further comprising an internal bus arrangement to couple shared resources in the processor to the plurality of microengines	
wherein the internal bus arrangement to couple shared resources, comprises:	wherein the internal bus arrangement to couple shared resources, comprises:
a translator device that translates requests from the general purpose processor to the microengines; and	a translator device that translates requests from the general purpose processor to the microengines; and
a first bus to couple the general purpose processor to the plurality of microengines; and	a first bus to couple the general purpose processor to the plurality of microengines; and
a second bus to couple the general purpose processor to the memory control system.	a second bus to couple the general purpose processor to the memory control system.

U.S. Patent 6, - Claim 15	*Application 10/615,500 - Claim 34*
The processor of claim 9	The processor of claim 28
further comprising an internal bus arrangement to couple shared resources in the processor to the plurality of microengines	

U.S. Patent 6, - Claim 15	*Application 10/615,500 - Claim 34*
wherein the shared resources comprise:	wherein the shared resources comprise:
a memory controller for controlling access to low latency memory;	a memory controller for controlling access to low latency memory;
a memory controller for controlling an access to high bandwidth memory;	a memory controller for controlling an access to high bandwidth memory;
a bus interface for controlling access to a communications bus; and	a bus interface for controlling access to a communications bus; and
a bus interface for controlling access to a computer bus.	a bus interface for controlling access to a computer bus.

Copending application 09/473,571 - Claim 33	*Application 10/615,500 - Claim 21*
A processor, comprising:	A processor comprises:
multiple multi-threaded programmable processing engines,	a plurality of microengines that support multiple hardware threads
individual ones of the programmable processing engines having at least one register; and an interface operationally coupled to the multiple programmable processing engines, the interface comprising: at least one register; and	
logic to: collect status data of at least one media access device via a bus, the status data indicating whether the at least one media access device has received packet data; and perform a transfer, unsolicited by the programmable processing engines, of at least a portion of the collected status data stored in the at least one register of the interface to at least one register of the multiple multi-threaded programmable processing engines.	a general purpose processor that coordinates system functions;

Copending Application 10/615,280 - Claim 16	*Application 10/615,500 - Claim 21*
A processor comprises:	A processor comprises:
a general purpose processor that coordinates system functions; and	a general purpose processor that coordinates system functions; and
a plurality of microengines that support multiple program threads,	a plurality of microengines that support multiple hardware threads.
each of the multiple engines having multiple program counters for different program threads provided by the respective engine, and operate on the network packets with a plurality of program threads to affect processing of the packets.	

Copending application 10/684,078 - Claims 1-3	*Application 10/615,500 - Claims 21,23*
A system comprising: a first port to receive a network packet; a second port in communication with the first port, the second port to transmit the network packet after processing; circuitry to associate first control information with a first portion of the network packet and to associate second control information with a second portion of the network packet; circuitry to process the first portion of the network packet and to process the second portion of the network packet at least partially in parallel with processing the firs t portion of the network packet; and circuitry to enqueue the first portion and the second portion for transmission to a second port in the same order in which the first portion and the second portion were received at the first port.	A processor comprises:

Copending application 10/684,078 - Claims 1-3	*Application 10/615,500 - Claims 21,23*
2. The system of claim 1 wherein the circuity comprises: one or more peripheral buses;	
a memory system;	(claim 23) The processor of claim 21 further comprising a memory control system.
a processor coupled to the one or more peripheral buses and the memory system,	a general purpose processor that coordinates system functions; and
the processor adapted to forward data from the first port to the second port; and a bus interface to receive the first portion of the network packet and the second portion of the network packet from the first port and enqueueing the first portion and the second portion in the order in which they were received from the first port for transmission to the second port, the first and second portions being processed at least partially in parallel.	
3. The system of claim 2 wherein the processor comprises one or more microengines to execute program threads,	a plurality of microengines that support multiple hardware threads.
the threads include receive schedule program threads to assign the first portion of the network packet from the first port to the first receive processing program thread and the second portion of the network packet to a second receive processing program thread, wherein the bus interface is responsive to the one or more microengines, and wherein the first and second receive processing program threads are adapted for processing and enqueueing.	

Copending application 10/726,757 - Claims 24, 27	*Application 10/615,500 - Claims 21, 23*

Copending application 10/726,757 - Claims 24, 27	*Application 10/615,500 - Claims 21, 23*
A processor comprising:	A processor comprises:
multiple multi-threaded engines integrated on a single semiconductor chip;	a plurality of microengines that support multiple hardware threads
a random access memory integrated on the same semiconductor chip; and	
a first memory controller integrated on the same semiconductor chip, the memory controller coupled to the random access memory and coupled to the multiple multi-threaded engines, the memory controller to receive and respond to commands issued by the multiple multi-threaded engines.	(claim 23) The processor of claim 21 further comprising a memory control system.
27. The processor of claim 24,	
further comprising a single-threaded processor integrated on the same semiconductor chip, the single-threaded processor having a different architecture than at least one of the multiple multi-threaded engines.	a general purpose processor that coordinates system functions

12 Claim 33 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-17 of U.S. Patent No. 6,606,704. Although the conflicting claims are not identical, they are not patentably distinct from each other because it would have been obvious to a person of ordinary skill in the art at the time the invention was made to duplicate parts for multiple effects and implement a third bus for connection to external bus interfaces. (*St. Regis Paper Co. v. Bemis Co.* 193 USPQ 8 (7th Cir. 1977)). Implementing an external interface would have been necessary for the system to perform any useful work because without an external interface, no information would have flowed in or out of the system. Implementing that external interface as a third bus would have been obvious for the motivating

reason that having a third independent bus would have allowed for data to flow in and out of the system independently of the level of utilization of the first and second busses.

13 The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14 The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

15 This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.

11 Claims 21, 23-24, and 27-35 are rejected under 35 USC 102(b) as being clearly anticipated by Wazlowski et al., *PRISM-II compiler and architecture*, IEEE Proceedings, Workshop on FPGAs for Custom Computing Machine, 1993.

Wazlowski et al. was cited as a prior art reference in applicant's information disclosure statement, paper number 20041226, received April 26, 2004.

Wazlowski et al. taught (e.g. see figs. 8) the invention as claimed (as per claim 21), including a data processing ("DP") system comprising:

11.1 a parallel hardware-based multithreaded processor (fig. 8) comprising:

11.2 a general purpose processor that coordinates system functions (fig. 8, "Am29050-33");

and,

11.3 a plurality of microengines ("Reconfigurable Array") that support multiple hardware threads (pg. 14, col. 1, lines 46-48).

12 As to claim 23, Wazlowski et al. taught a memory control system (fig. 8, "Burst-Mode Memory Controller").

13 As to claim 32, Wazlowski et al. taught an internal bus arrangement to couple shared resources (fig. 8) comprising:

a translator device that translates requests from the general purpose processor to the microengines ("coprocessor interface");

a first bus to couple the general purpose processor to the plurality of microengines ("Data bus"); and,

a second bus to couple the general purpose processor to the memory control system ("address bus").

14 As to claim 24, Wazlowski et al. taught that the memory control system comprised a synchronous dynamic random access memory controller ("Burst-Mode Memory Controller", "DRAM") that sorts memory references based on whether the memory references are directed to an even bank or an odd bank of memory ("Interleaved DRAM Bank A", "Interleaved DRAM Bank B").

15 As to claims 27-28, Wazlowski et al. did not show a high speed bus interface that couples the processor to a communication bus or that couples to a processor system bus, however it is inherent that such a bus interface must have been provided in order to communicate with the system, because without one, the system is isolated and does not perform any useful work.

16 As to claim 34, Wazlowski et al. taught a memory controller for controlling access to low latency memory ("cache", a cache controller must inherently be present for the cache to function);

a memory controller for controlling an access to high bandwidth memory ("Burst-Mode Memory Controller"); and,

the claimed bus interfaces are inherent for the same reasons presented as to claims 27-28, supra.

17 As to claim 29, Wazlowski et al. taught an internal bus arrangement to couple shared resources in the processor to the plurality of microengines (fig. 9).

18 As to claim 30, Wazlowski et al. taught a first bus to couple the general purpose processor to the plurality of microengines ("Data Bus").

19 As to claim 31, Wazlowski et al. taught a translator device that translates requests from the general purpose processor to the microengines ("coprocessor interface");

a first bus to couple the general purpose processor to the plurality of microengines ("Data bus").

20 As to claim 33, Wazlowski et al. inherently would contain a third bus to couple the microengines to an external interface for the reason presented as to claims 27-28, supra.

21 As to claim 35, Wazlowski et al. did not specifically teach a program counter per microengine. However, as the definition of multithreaded indicates that one of the state values associated with a thread is a program counter value, it would be inherent that a system for processing independent tasks in each engine (pg. 14, col. 1, lines 46-49) would also necessarily need independent program counters for those tasks that are based on operations relying on a

program counter value.

22 Claim 25 is rejected under 35 USC § 103 as being unpatentable over Wazlowski et al. as applied to the preceding claims.

23 As to claim 25, Wazlowski et al. taught a static random access memory controller ("cache", a controller must inherently be provided). Wazlowski et al. did not teach that the memory controller sorts memory references based on reads vs. writes. However, it is notoriously well known in the art that read requests are significantly more critical than write requests because for read requests the processor is waiting while the read is serviced, whereas writes can be buffered and serviced asynchronously to processor operation and official notice of such is hereby taken. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have sorted memory requests based on reads vs. writes because of the well known speed and performance critical nature of reads over writes. Doing so would have further increased the performance of the system.

24 Claim 26 is rejected under 35 USC § 103 as being unpatentable over Wazlowski et al. in view of Trimberger et al., *A time-multiplexed FPGA*, IEEE Proceedings of The 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997.

Trimberger et al. was cited as a prior art reference in applicant's information disclosure statement, paper number 20040426, received April 26, 2004.

25 As to claim 26, Wazlowski et al. did not teach that each of the microengines employed hardware-based context swapping amongst a plurality of threads that are independently executable within each of the microengines. However, Trimberger et al. taught a system for allowing individual FPGAs to perform hardware-based context swapping for the purpose of

swapping amongst a plurality of threads each independently executable on the FPGA (pg. 23, specifically the paragraph titled "Time Share Mode"). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have replaced Wazlowski et al.'s conventional FPGAs with Trimberger et al.'s time-multiplexed FPGAs because of Trimberger et al. teaching that time-multiplexing an FPGA produces several independent virtual FPGAs and provides greater utilization of the hardware resources (pg. 22, section titled "The Basic Concept" and pg. 23, paragraph titled "Time Share Mode").

26 Claim 22 is rejected under 35 USC § 102(b) as clearly anticipated by or, in the alternative, under 35 USC § 103 as obvious over Wazlowski et al. as applied to claim 21, supra.

27 As to claim 22, Wazlowski et al. did not specifically teach that the general purpose processor loaded microcontrol programs in the plurality of microcontrol engines. However, as seen from the figure of the hardware platform (figure 8) it is seen that the connection to the microcontrol engines is only shown as originating from the general purpose processor. Therefore, it would be inherent from the drawing shown that the microcontrol programs would be loaded into the microcontrol engines via the general purpose processor busses and therefore by the general purpose processor itself. However, in the case where it might not be inherent, it clearly would have been obvious to a person of ordinary skill in the art at the time the invention was made to have utilized the general purpose processor for loading of microcontrol programs into the microengines because the general purpose processor has already been provided and interconnected for operation with the microcontrol engines and therefore use of this processor to load microcontrol programs would reduce the overall cost of the system by preventing the need to create a wholly separate system for loading microcontrol programs into the microengines.

One of ordinary skill in the art would be motivated to build the system this way because Wazlowski et al. indicates that one of the objectives of the system was cost-effectiveness (pg. 11, col. 1, last bullet point).

28 A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

29 Any inquiry concerning this communication or earlier communications from the Examiner should be directed to RichardEllis whose telephone number is (571) 272-4165. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (571) 272-4162. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Richard Ellis
March 15, 2005

RICHARD L. ELLIS
PRIMARY EXAMINER